USTHB : computer Science Faculty — May, 10, 2025

1st year Licence en computer Science — Correction of the final exam (STRM2.)

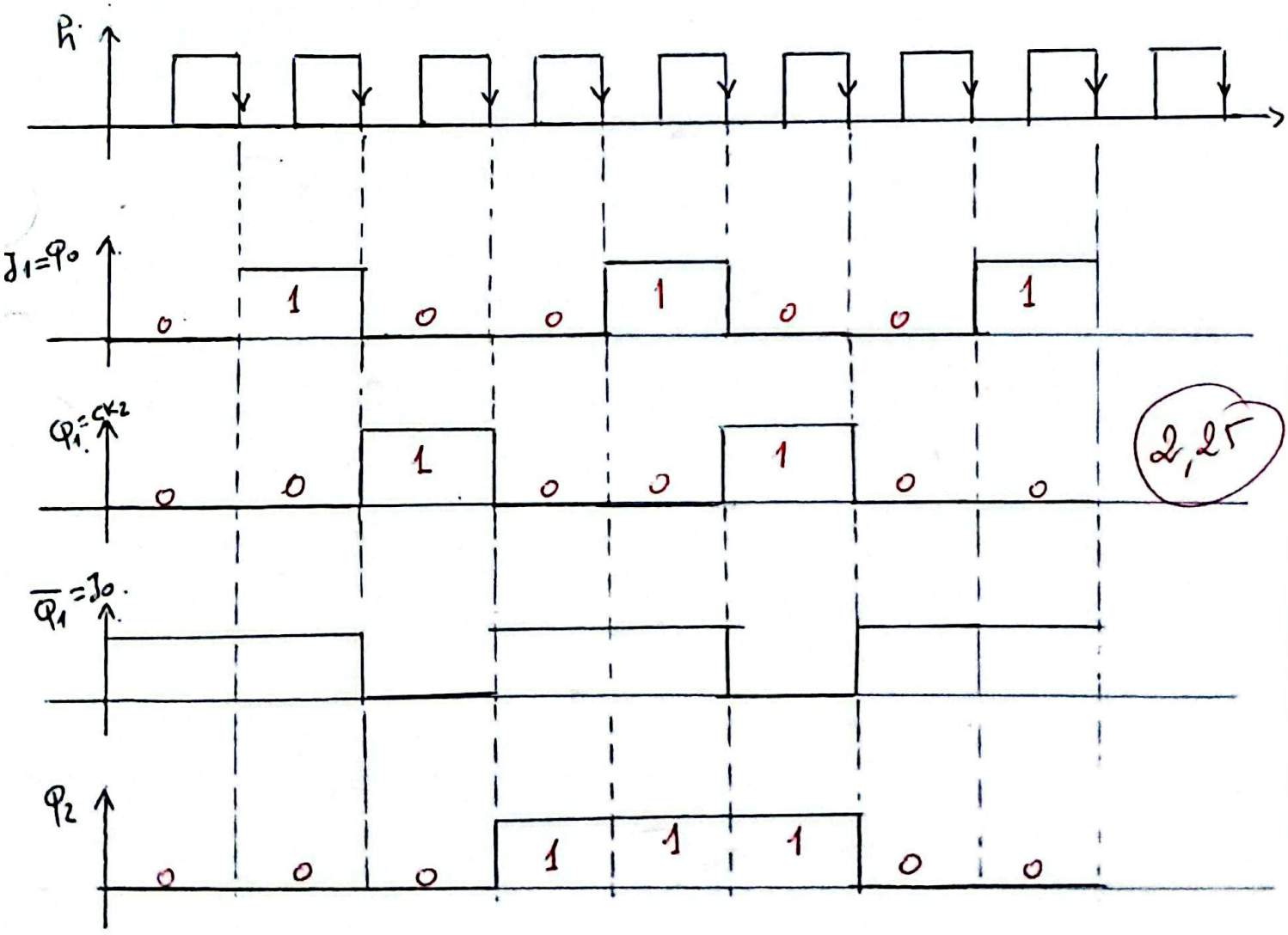
Exercise 1

1.1) the equations of the flip-flop inputs.

$$\begin{cases} J_0 = \overline{Q_1} \\ K_0 = 1 \\ CK_0 = h \end{cases} ; \begin{cases} J_1 = Q_0 \\ K_1 = 1 \\ CK_1 = h \end{cases} ; \begin{cases} J_2 = 1 \\ K_2 = 1 \\ CK_2 = Q_1 \end{cases}$$

0,25 0,25 0,25

1.2 The corresponding chronogram



1.3 The sequence performed:

000 → 001 → 010 → 100 → 101 → 110 (1)

2) 2.1 sequence : $1 \to 5 \to 7 \to 2 \to 3 \to 1 \to \dots$

$000 \to 101 \to 111 \to 010 \to 011 \to 001 \to \dots$

Table of excitement :

Q_2	Q_1	Q_0	Q_2^+	Q_1^+	Q_0^+	D	T	J_0	K_0
0	0	1	1	0	1	1	0	X	0
1	0	1	1	1	1	1	1	X	0
1	1	1	0	1	0	0	0	X	1
0	1	0	0	1	1	0	0	1	X
0	1	1	0	0	1	0	1	X	0

1,5

2.2) Simplified equations with Karnaugh-map.

D.

Q_2 \ Q_1Q_0	00	01	11	10
0	X	1	0	0
1	X	1	0	X

$D = \overline{Q_1}$ 0,5

T

Q_2 \ Q_1Q_0	00	01	11	10
0	X	0	1	0
1	X	1	0	X

$T = \overline{Q_2}Q_1Q_0 + Q_2\overline{Q_1}$ 0,5

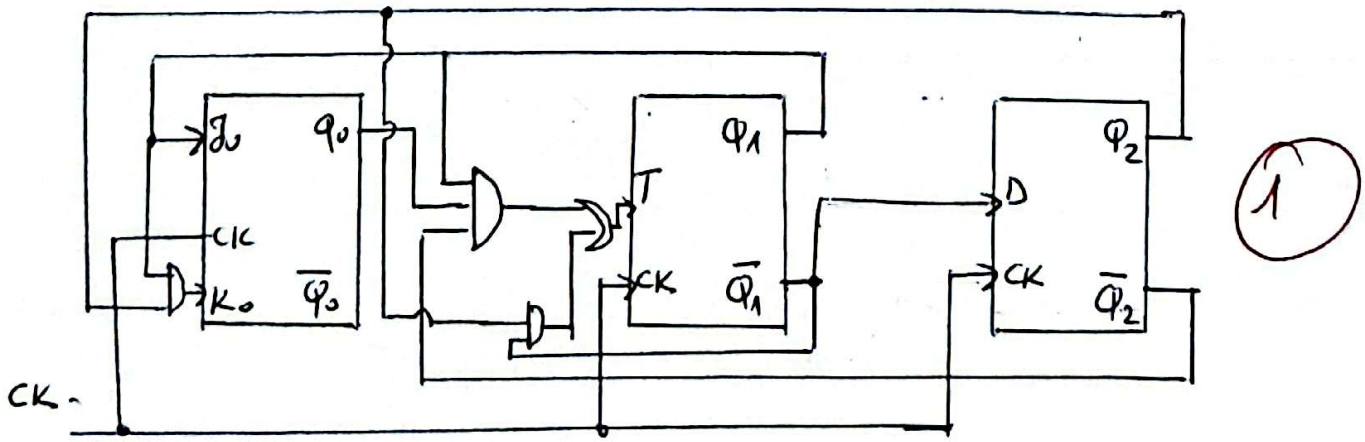
from the table we deduce that:

$J_0 = Q_1$ 0,25

K_0

Q_2 \ Q_1Q_0	00	01	11	10
0	X	0	0	X
1	X	0	1	X

$K_0 = Q_2Q_1$ 0,25



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Exercise 2:

Machine with: 32 bit address bus
32 bit data bus.
main memory 12 GB { RAM = 8 GB, ROM = 4 GB }

capacity on word / word = 4B.

RAM: $\frac{8\,GB}{4B} = 2G \times 4B$.

ROM: $\frac{4\,GB}{4B} = 1G \times 4B$

~~Har~~ Type of hardware in the store:

Blocks RAMi: 4 GB with word of 16 bit

$RAM_i = \frac{4\,GB}{2B} = 2G \times 2B$

Number of RAMi to be placed in series:

$N = \frac{2G \times 4B}{2G \times 2B} = 2 \Rightarrow 2\,RAM_i = (RAM_1 + RAM_2)$ (0,5)

Blocks ROMi: 2 GB with word of 32 bit

$ROM_i = \frac{2\,GB}{4B} = 0,5G \times 4B$

Number of ROMi to be placed in parallel:

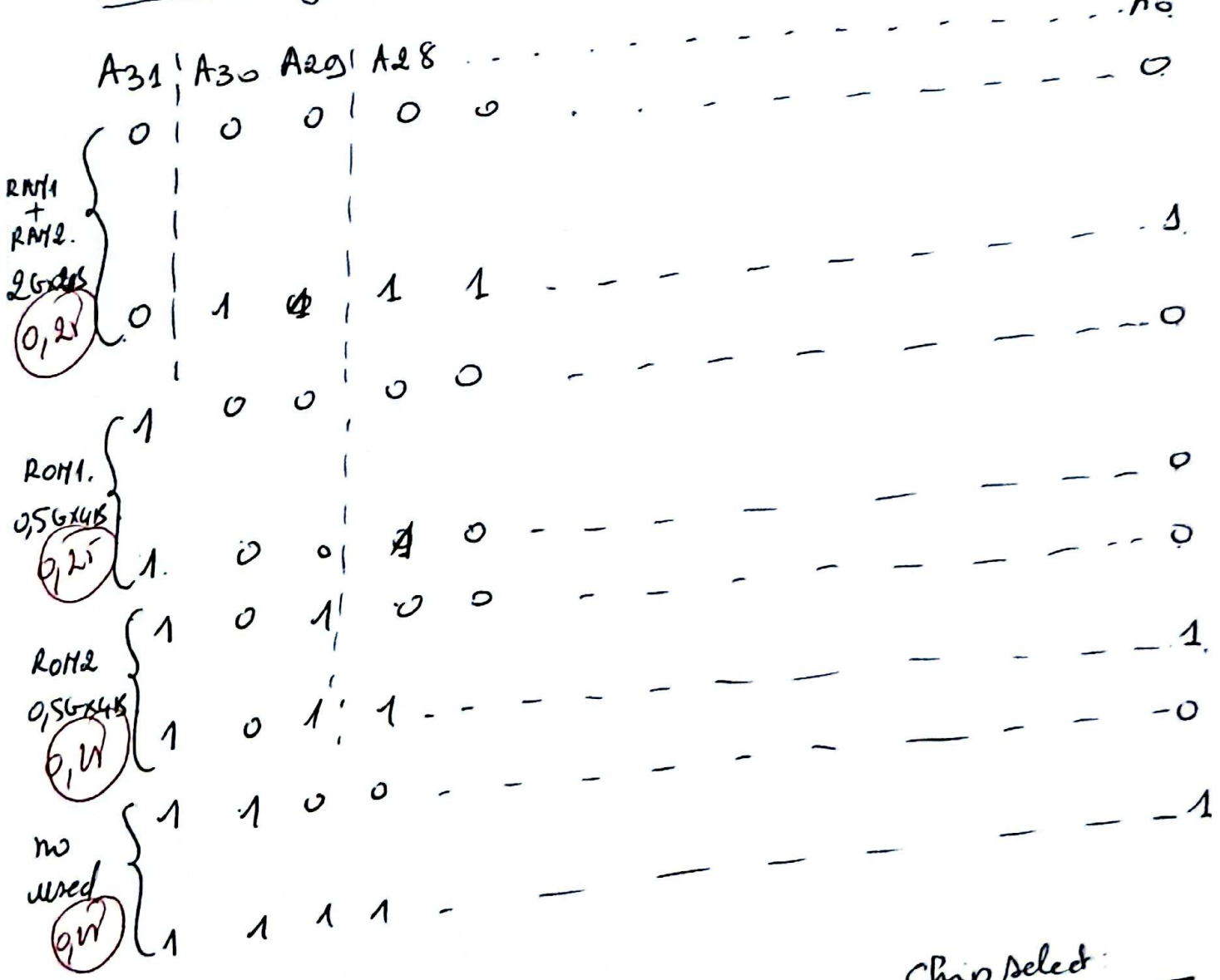
$N = \frac{1G \times 4B}{0,5G \times 4B} = 2 \Rightarrow 2\,ROM_i\ (ROM_1 + ROM_2)$ (0,5)

To address the RAMi of 2G, we need n address lins such $2^n = 2G = 2 \cdot 2^{30} = 2^{31} \Rightarrow$ n = 31 lins (0,25)

To address the ROM1 or ROM2 of 0,5 G, we need n address lins / $2^n = 0,5G = 2^{-1} \cdot 2^{30} = 2^{29} \Rightarrow$ n = 29 lins. (0,25)

2) Connection diagram of these blocks and their address ranges.

Address ranges:



Address range of RAM1 + RAM2.

0,W [00000000, 07FFFFFF].

Chip Select:

$CS_{RAM_1} = CS_{RAM_2} = \overline{A_{31}}$ 0,W

Address range of ROM1:

0,W [80000000, 9FFFFFFF]

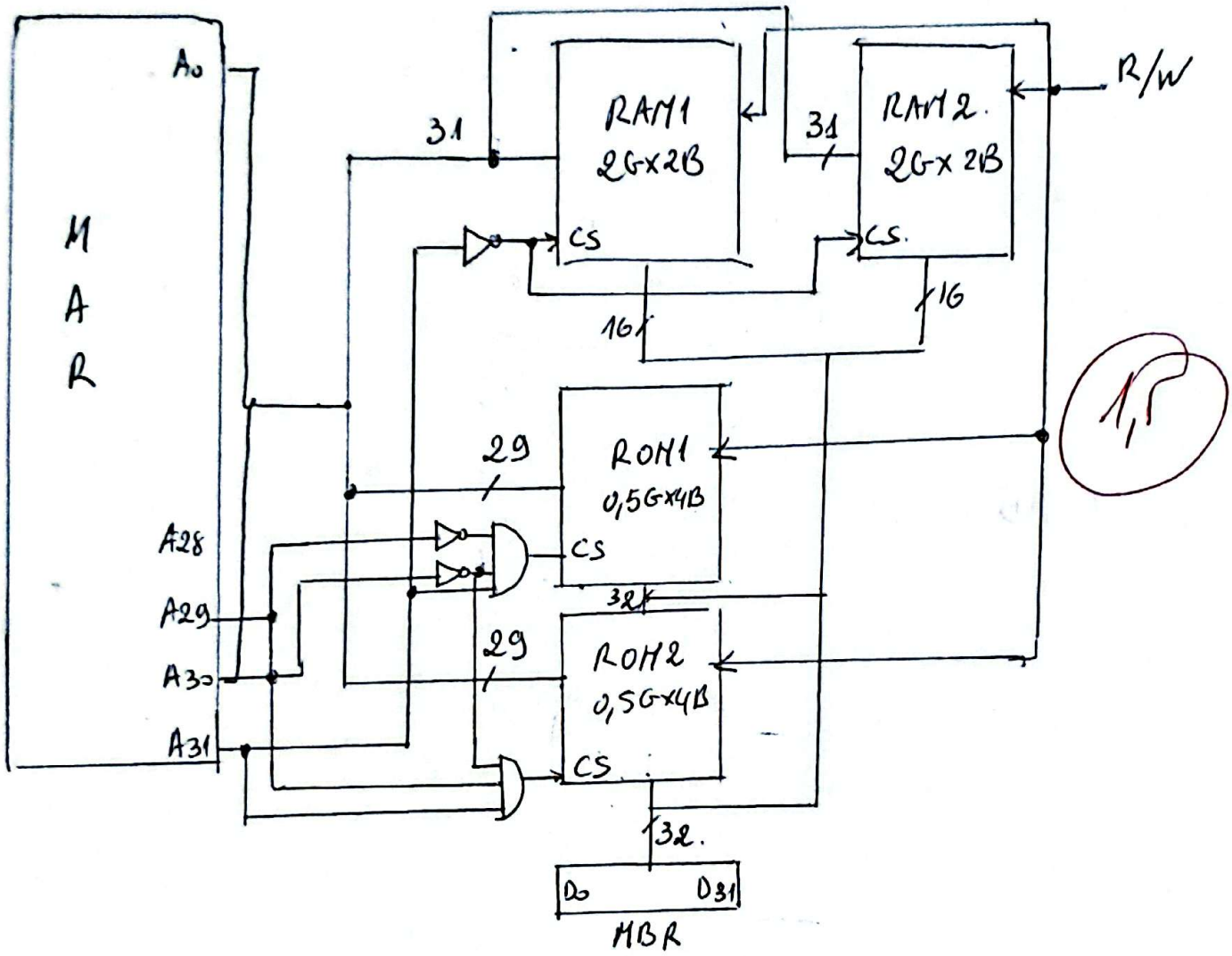
$CS_{ROM_1} = A_{31}\overline{A_{30}}A_{29}$ 0,W

Addrss range of ROM2:

0,W [A0000000; BFFFFFFF].

$CS_{ROM_2} = A_{31}\overline{A_{30}}A_{29}$ 0,W

Connections



3) yes this memory is expandable.

From the previous ~~range address~~ address range, It remains the following address range

[00000000, FFFFFFFF]

0,5

so;

FFFFFFFF
- 00000000
3FFFFFFF
+ 1
40000000

so, $(40000000)_{16} = 2^{30} = 1G$.

expandable by

1G×4B

Exercise 3:

101 LOAD 0, IMM Acc ← 0 ; Acc = 0 XRI

102 STORE XRI (XRI) ← Acc = 0 ; Acc = 0; XRI = 0.

103 LOAD 300, XRI : Acc ← (300 + XRI) = (300) = A ; Acc = A ; XRI = 0

104 MUL 400, IND : Acc ← Acc * ((400)) = Acc ← A * A ; XRI = 0

105 STORE 303, XRI : (XRI + 303) ← (Acc) ; (303) ← A^2

106 LOAD 1, IMM : Acc ← 1 ; Acc = 1 ; XRI = 0.

107 STORE, XRI XRI ← (Acc) = 1 ; XRI = 1 , Acc = 1.

108 LOAD 301, D Acc ← (301) = B ; Acc = B ; XRI = 1.

109 MUL 301, D Acc ← Acc * (301) = B^2 XRI = 1

110 ADD 302, XRI Acc ← Acc + (302 + XRI) = $B^2 + A^2$

111 STORE 303, D (303) ← Acc = $B^2 + A^2$.

112 MUL 302, XRI Acc ← Acc * (302 + XRI) = $(B^2 + A^2)$ * (303)
= $(B^2 + A^2) \cdot (B^2 + A^2)$

113. STORE 303, D. (303) ← Acc = $(B^2 + A^2)^2$.

114 LOAD 5, IMM Acc ← 5 ; Acc = 5

115 ~~LOAD~~ STORE XRI XRI ← (Acc) = 5 ; Acc = 5, XRI = 5.

116 LOAD 297, XRI Acc ← ~~(302)~~ (297 + 5) = (302) = C.

117 MUL 302, D Acc ← Acc * (302) = C * C = C^2

118 STORE Y, D (Y) ← Acc = C^2 XRI = 5.

119 LOAD 298, XRI Acc ← (298 + 5) = (303) = $(B^2 + A^2)^2$.

120 DIV Y, D Acc ← Acc / (Y) = $\frac{(B^2 + A^2)^2}{C^2}$.

121 STORE 303, D (303) ← Acc = $\frac{(B^2 + A^2)^2}{C^2}$

122 Write ~~Affichage~~ display $\frac{(B^2 + A^2)^2}{C^2}$

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2) This program calculates the following equation :

$$\frac{(B^2+A^2)^2}{C^2}$$ (0,5)

3) Execution phase of the instruction with CO = 104.

Phase1 : (Find the instruction to be processed)

Put the contents of the CO = 104 in the MAR MAR ← 104.

Memory read command (R/W = 1) (0,5)

Transfer MBR contents to the RI register RI ← MUL 400, [MBR].

Analysis and decoding.

Phase2 : (decoding and processing).

Transfer of operand address 400 to the MAR (MAR ← 400).

Reading control (R/W = 1).

Transfer of MBR contents to MAR MAR ← (MBR) = 300. (0,75)

Reading control (R/W = 1).

Transfer of MBR content to the ALU : MBR = A → ALU

Control of operation execution (Multiplication) : Acc ← Acc × A

Acc ← A^2

Phase3 : (go to next instruction)

CO ← CO + 1. (0,25)